Bipolar Dynamic Memory Cell

HORST H. HENN

Abstract—**A bipolar dynamic memory cell for use in a high-speed random-access memory consists of a cross-coupled pair of transistors and two diodes. Information is dynamically stored using a bistable charge distribution and must be refreshed at a frequency of 1 kHz by a SELECT operation. Standby power per memory cell is in the nanowatt range. The cell requires only 3 interconnect lines and can be fabricated with standard bipolar technology on 12-mil² silicon area. Cycle time is limited by the speed of decoding, driving, and sensing circuits and is estimated to be 50 ns for a 512-bit RAM chip with complete on-chip decoding.**

Introduction

HIGH-SPEED operation, low cost, high capacity, and low standby power are essential goals of LSI random-access memory development. However, neither MOS nor bipolar technology, commonly used for memory realizations, can provide all these features together.

MOS technology offers small memory-cell size, low standby power, and low cost [1]. High-speed operation seems not to be possible with all-MOS designs due to low speed of MOS decoding, driving, and sensing circuits. Combining MOS memory cells and bipolar interface circuitry results in higher speed, but causes severe interconnection problems because MOS and bipolar circuitry cannot be fabricated economically on the same chip.

Bipolar technology enables high-speed operation. Unfavorably, standby power of commonly used bipolar flip-flop cells is high. Only low-valued resistors can be realized with standard fabrication processes on small silicon area. With sophisticated technology load-resistors of bipolar flip-flops can be increased without enlarging cell size [2], [3]. However, further size and complexity reduction of bipolar memory cells is highly desirable.

Another approach to standby power reduction of memory cells that also provide small cell size is dynamic operation. In dynamic memory cells information is stored in the form of a charge. This charge always tends to leak off and must be refreshed periodically. Standby power of dynamic memory cells is extremely low and is determined mainly by the refresh frequency necessary for stable information storage.

In this paper, a dynamic bipolar memory cell for use in a high-speed random-access memory is described. Charge-holding and regeneration capability of a diode-isolated flip-flop have been combined to achieve dynamic information storage with bipolar devices. The main advantage of this approach is that the cell need not contain any resistors although its standby power is in the nanowatt range. Noncritical fabrication with standard technology and significant cell-size reduction due to decreased cell complexity are possible. The high-speed performance advantage of bipolar circuitry is not sacrificed. Feasibility is proven for this operation mode of bipolar circuitry and a proposed memory array is described.

Manuscript received April 5, 1971; revised June 1, 1971.
The author is with the Institut fuer Nachrichtentechnik, Stuttgart University, Stuttgart, Germany.

Charge-Controlled Flip-Flop Operation

The memory cell proposed here and illustrated in Fig. 1 uses the charge-holding capability of bipolar transistors. For the sake of demonstration, the charge distributed in the cross-coupled pair of transistors [4] is assumed to be concentrated on two node capacitances C_{N1} and C_{N2}.

The nominal operation of the memory cell is as follows. Suppose V_C is raised to 2.5 V and transistor T_1 is initially ON, a certain amount of charge is stored on the node capacitance C_{N2}. On the other hand there is far less charge stored on C_{N1}. When V_C is pulled to ground the coupling diodes are reverse biased, causing short reverse currents to flow, which can be neglected for first-order estimation. The cross-coupled pair of transistors subsequently is isolated from the peripheral circuitry. Charge stored on the node capacitance C_{N2} is diminished by the forward current via the emitter–base junction of T_1 and additional leakage currents. If V_C is raised again to 2.5 V, the node capacitances C_{N1} and C_{N2} are charged up simultaneously and the node voltages V_1 and V_2 increase. Due to the charge initially stored on C_{N2}, the node voltage V_2 is at any time higher than V_1. Therefore, transistor T_1 reaches its active state before T_2. Resulting collector current flowing in T_1 forces the memory cell to its initial state with T_1 ON and T_2 OFF.

This STORE–REFRESH cycle is shown in Fig. 2 as a loop in the V_1, V_2 state plane, which characterizes dynamical stability [5]. The outer points of intersection of the voltage-transfer characteristics $V_1(V_2)$ and $V_2(V_1)$, which are only skeletonized, yield the two stable points P_0 and P_1 for static operation. When V_C is pulled down to ground the STORE path is swept with decreasing speed. Refresh takes place at state R. The REFRESH path will never cross the separatrix, resulting in final state P_0 and loss of information, if R is situated below the separatrix [6]. Thus, the final state of the memory cell is controlled by the difference of node voltages V_1 and V_2, which is equivalent to the difference of charges stored on C_{N1} and C_{N2}. In a real memory cell this voltage difference should not fall below a critical value, e.g., 100 mV during STORE to ensure proper operation in spite of manufacturing varia-

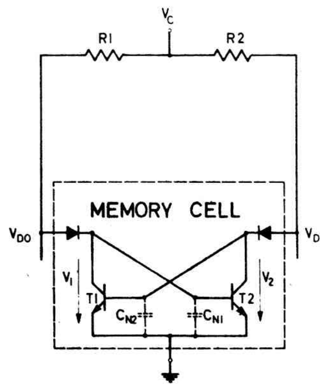

Fig. 1. Charge-controlled flip-flop.

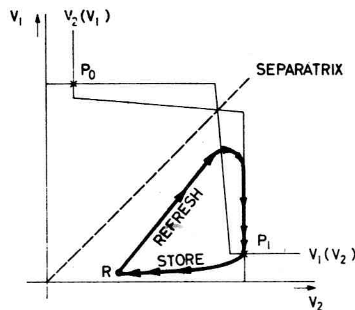

Fig. 2. STORE-REFRESH cycle of charge-controlled flip-flop.

tions and noise. Fig. 3 demonstrates that the difference of node voltages can exceed 100 mV for more than 100 ms. (Measurement was taken using high-input-impedance MOSFET amplifiers with voltage gain equal to unity to avoid additional leakage currents.) Therefore, frequency at which stored charge must be refreshed can be very low.

Due to the cell's inherent bistability during STORE and REFRESH operations good noise immunity and common-mode rejection are achieved. Note that a charge distribution, once established, is self-refreshing. No time-consuming and noise-sensitive READ-WRITE cycle is necessary. READ and WRITE operations of the charge-controlled flip-flop do not differ much from those of a conventional static flip-flop in regard to access, signal levels, and speed. For READ, V_C is raised to 2.5 V and V_{D0} and V_{D1} are differentially sensed. For WRITE, either V_{D0} or V_{D1} are pulled to 1 V and V_C is raised to 2.5 V, resulting in current flowing only to transistor T_1 or T_2. Time required for REFRESH of stored charge typically is below 5 ns for an integrated flip-flop. The regenerative gain of a flip-flop has been widely used in high-speed comparators for strobed interrogation of a difference voltage [7].

Refresh Considerations

Performance of dynamic memories is strongly affected by the frequency at which information must be refreshed. If the frequency is high, many memory cycles are wasted for refresh and the virtual speed of memory is slowed down. Beyond that, standby power is in straight-line proportion to refresh frequency. As has been pointed

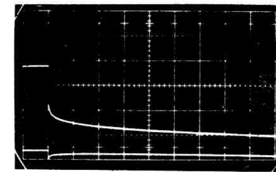

Fig. 3. Node voltages of a charge-controlled flip-flop during STORE—0.2 V, 10 ms/div. Transistors—CA 3046. diodes—CA 3039; substrate was held at −3 V.

out, the difference of node voltages should not fall below a critical value to ensure proper operation in spite of manufacturing variations and noise. Refresh frequency measurements with nonmatched devices indicate that stable information storage is possible unless the difference of node voltages falls below 10 mV in noiseless or 100 mV in noisy environments. Therefore, refresh frequency evaluations are based on a minimum node voltage difference of 100 mV.

Charge-holding capability of charge-controlled flip-flop can be investigated using the simple diode model shown in Fig. 4(a). When switch S is opened, the node capacitance C_N is discharged by the forward current I_F via the emitter–base junction and additional leakage currents, causing a decrease of node voltage V. For silicon diodes a good representation of the forward current–voltage characteristics is

$$I_F = I[\exp(qV/kT) - 1]. \tag{1}$$

According to Fig. 4(a) the following nonlinear differential equation results

$$\frac{dV}{dt} + \frac{I}{C_N}[\exp(qV/kT) - 1] = 0. \tag{2}$$

Integration of (2) yields

$$v(t) = -\frac{kT}{q} \ln [1 + \{\exp[-qV(0)/kT] - 1\} \exp(-t/\tau)] \tag{3}$$

$$\tau = kTC_N/qI \tag{4}$$

where $V(0)$ is the forward bias initially applied to the emitter–base junction and τ a time constant, which is almost independent of device size. This time constant depends on layout and fabrication of the charge-controlled flip-flop and is, with its greater capacitance, somewhat longer than that of a single emitter–base junction used for measurements and computations. For standard p-n junctions τ is typically 10 s at 20°C. Unfortunately, τ is highly temperature dependent due to the current I; its temperature dependence is approximately the same as that of n_i^2 [8]. However, voltage decay of a standard p-n junction shown in Fig. 4(b) indicates that node voltage V can exceed 100 mV for a couple of milliseconds, even at 70°C, in spite of fast initial decay. Thus, refresh frequency of about 1 kHz is sufficient for operation over the temperature range of 0–70°C. Keeping within this tem-

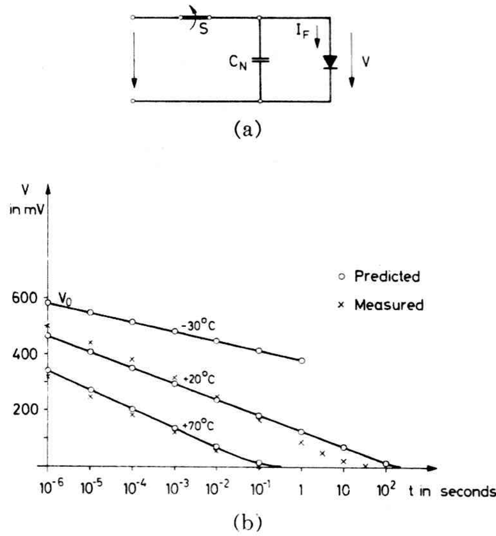

Fig. 4. Voltage decay of forward-biased p-n junction. (a) Charge-holding model. (b) Measured–predicted voltage versus time for a CA 3046 emitter–base junction.

perature range is favored for low standby power of dynamic memory cells.

Memory Array Organization

A block diagram of a 512-bit chip is shown in Fig. 5. Fast on-chip decoding and sensing are possible with bipolar circuits, which do not differ from that of standard bipolar memories. The nominal operation of the proposed two-dimensional array is as follows. In the standby condition all word lines are held at approximately 3 V and the digit lines at 2.5 V. All coupling diodes are reverse biased and information is dynamically stored in the cells. For SELECT one word line is pulled down forward biasing the coupling diodes of all cells tied to this line. Currents flowing through the memory cells discharge the digit line capacitances. A current of 0.5 mA flowing through the ON transistor provides a 100-mV readout in 2 ns with a total capacitance per digit line of 10 pF. Margin maximally obtained is approximately 1.4 V. In a real memory cell, this margin is lowered by parasitic resistances in diodes and transistors much alike in diode-coupled static flip-flop cells. Nevertheless, worst case margin of 200 mV can be expected [3]. To read out the information stored in a cell, a pair of digit lines is differentially sensed after SELECT. For WRITE one digit line is raised and the other digit line is pulled down together with the word line, forcing the cell to its new state. Fast WRITE is achieved because the cell can be operated at high current level.

The array of memory cells has two outstanding features resulting in substantial silicon-area savings. Only two low-valued resistors per column are necessary; the cells themselves do not contain any resistors. Three interconnect lines are sufficient for random-access operation. Thus, single-layer metalization is possible with a small number of crossunders.

The node voltages of the memory cell track with word line voltage as long as the coupling diodes are reverse

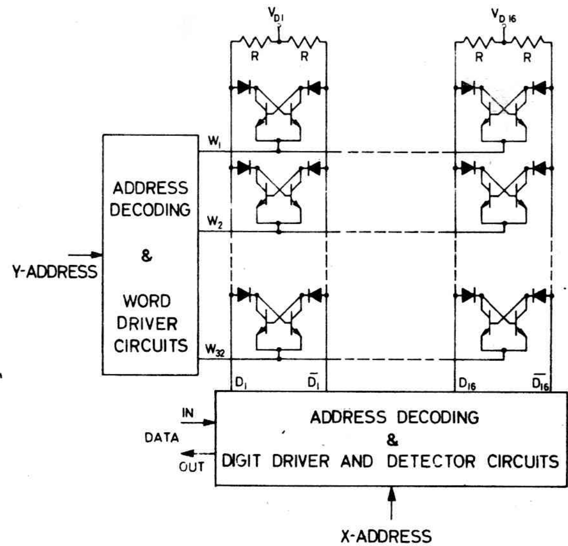

Fig. 5. Block diagram of a 512-bit RAM chip.

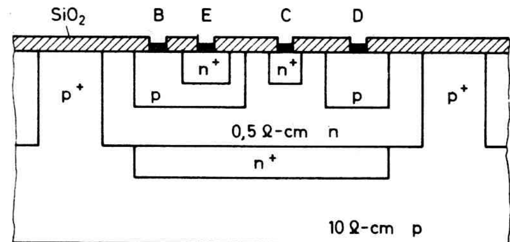

Fig. 6. Cross section of integrated transistor and coupling diode.

biased. Therefore, a single memory cell can also be activated in the array by applying appropriate voltages to the word lines and via the load resistors R to the digit lines. If very high speed is intended, SELECT of a single cell enables driving this cell with great currents. However, activating a row of cells by a SELECT operation is preferred so as to refresh with a single memory cycle all cells tied to a common word line. With some additional circuitry the two operation modes can also be combined.

Integration and Performance

A charge-controlled flip-flop is composed of devices consisting of a transistor and a coupling diode. These devices can be fabricated, for instance, by adding a high-quality Schottky-barrier diode to a standard diffused transistor [2], [3]. Although leakage currents of these Schottky-barrier diodes are in the nanoampere range, stable information storage can be achieved at a refresh frequency of about 10 kHz. However, it is felt that large arrays can only be fabricated with well-established LSI-fabrication techniques. Additional critical production steps must be avoided. Therefore, the structure shown in Fig. 6 is proposed. A charge-controlled flip-flop cell based on this structure occupies about 12-mil² silicon area if contemporary tolerances of 0.4-mil linewidths and 0.2-mil spacings are chosen. For comparison, a static bipolar flip-flop cell using the same tolerances requires about 30 mil². Dynamic instead of static operation allows doubling

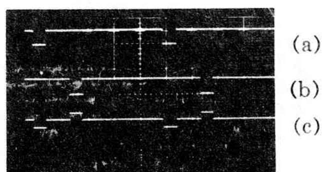

Fig. 7. REFRESH of two cells. Horizontal scale: 20 ms/div. (a) WORD SELECT 1—5 V/div. (b) WORD SELECT 2—5 V/div. (c) Differential signal on the digit lines—0.5 V/div.

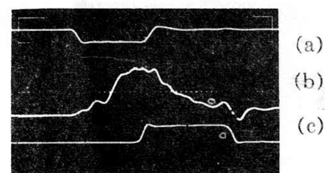

Fig. 8. READ of charge-controlled flip-flop. Horizontal scale: 10 ns/div. (a) WORD SELECT—5 V/div. (b) Differential signal on the digit lines—0.2 V/div. (c) DATA OUT—5 V/div.

of cells per chip without enlarging chip size. Beyond that, decrease of cell complexity will result in higher yield. Therefore, a 512-bit dynamic RAM chip seems to be feasible with contemporary technology.

For the sake of demonstration, a memory model according to Fig. 5 was realized. The memory cells are composed of transistor and diode arrays. Fig. 7 illustrates alternate refreshing of two cells that have common digit lines. Stable information storage at a refresh frequency of 10 Hz is demonstrated ($T = 20°C$). High-speed operation of a charge-controlled flip-flop is shown in Fig. 8. The cell provides a signal on the digit lines of 100 mV in 10 ns. This signal is differentially sensed and stored with aid of a diode-isolated flip-flop [7], which does not need any standby power. The additional delay introduced by dynamic instead of static operation of the memory cell is approximately 5 ns. In an integrated array it is even shorter due to reduced RC time constants. This delay scarcely affects memory-system performance. WRITE time of a charge-controlled flip-flop is shorter than that of an equivalent static flip-flop because no static base current is supplied to the transistor to be turned off. At 20 MHz READ-WRITE, the experimental cell's WRITE time is 20 ns. This time is mainly limited by saturation charge stored in the transistor previously ON. Reverse current flowing through the coupling diodes can extract a good deal of this charge. Thus, use of p-n junctions for these diodes is favorable.

The coupling diodes of the proposed memory cell differ somewhat from the diodes used in the experimental model. Parasitic substrate p-n-p transistor action is quite harmful for static operation. Because switching speed of the p-n-p transistor, being slow compared with speed of the narrow-base n-p-n transistor, dynamic operation is little affected. Moreover, the current gain of the p-n-p transistor can be lowered by gold doping. The charge-holding capability of the charge-controlled flip-flop is not affected at all by parasitic p-n-p transistor action.

The expected performance data of the proposed memory array are as follows. Refresh frequency of 1 kHz is sufficient for 0–70°C operation. Since the cell is activated only for 10 ns for REFRESH, its standby power is only 10 nW if the standby power of the equivalent static flip-flop is 1 mW. Speed of a 512-bit RAM chip is mainly limited by the speed of decoding, driving, and sensing circuits. With gold doping or Schottky-barrier-diode antisaturation clamps for peripheral circuitry [9], READ or WRITE cycle time is estimated to be 50 ns or less. All memory cells of a 512-bit chip can be refreshed with 32 memory cycles. Thus only 0.16 percent of memory cycles are wasted for refresh of the stored information.

Summary and Conclusions

A memory cell has been described that uses charge-holding capability of bipolar devices for dynamic information storage. Refresh of the stored charge is achieved by a SELECT operation; no READ-WRITE cycle is necessary. The percentage of memory cycles wasted for refresh is less than that of dynamic MOS memory cells. Noncritical processing, low standby power, and halved cell size compared to equivalent static flip-flop cells should permit fabrication of high-speed bipolar random-access memories at significantly reduced cost.

Acknowledgment

The author would like to thank Prof. G. Kohn for helpful discussions and constant encouragement, J. Eberspaecher, H. Guendner, and H. Roesch for stimulating discussions, and H. Rau, who did a good deal of experimental circuit investigations.

References

[1] W. M. Regitz and J. A. Karp, "Three-transistor-cell 1024-bit 500-ns MOS RAM," *IEEE J. Solid-State Circuits*, vol. SC-5, Oct. 1970, pp. 181–186.
[2] D. A. Hodges *et al.*, "Low-power bipolar transistor memory cells," *IEEE J. Solid-State Circuits*, vol. SC-4, Oct. 1969, pp. 280–284.
[3] D. J. Lynes and D. A. Hodges, "Memory using diode-coupled bipolar transistor cells," *IEEE J. Solid-State Circuits*, vol. SC-5, Oct. 1970, pp. 186–191.
[4] J. J. Sparkes, "A study of the charge control parameters of transistors," *Proc. IRE*, vol. 48, Oct. 1960, pp. 1696–1705.
[5] W. J. Cunningham, *Introduction to Nonlinear Analysis*. New York: McGraw-Hill, 1958, ch. 10.
[6] G. Kohn, "Die Beschreibung des Umklappvorganges beim Multivibrator," *Arch. Elek. Übertragung*, vol. 14, May 1960, pp. 193–203.
[7] W. C. Slemmer, "High-speed low-power strobed comparator," *IEEE J. Solid-State Circuits*, vol. SC-5, Oct. 1970, pp. 215–220.
[8] A. S. Grove, *Physics and Technology of Semiconductor Devices*. New York: Wiley, 1967, ch. 6.
[9] J. C. Barett *et al.*, "Design considerations for a high-speed bipolar READ-ONLY memory," *IEEE J. Solid-State Circuits*, vol. SC-5, Oct. 1970, pp. 196–202.

Reprinted by permission from
IEEE JOURNAL OF SOLID-STATE CIRCUITS
Vol. SC-6, No. 5, October 1971
Copyright © 1971, by the Institute of Electrical and Electronics Engineers, Inc.
PRINTED IN THE U.S.A.